Abstract

Advances in power electronics materials continue to push the boundaries on high temperature operation of electronic packaging constituents. Wide bandgap semiconductors that operate at higher temperature are becoming more available and cycling lifetimes of substrates and die attach materials continue to increase. However, the real challenge is still implementation of a package capable of harnessing the improvements of each component. Electronic packages in applications like electric vehicles (PHEV/HEV/EV) and alternative energy conversion are exposed to large thermal stresses due to challenges of providing sufficient cooling without reductions in overall system efficiency. An innovative package that reduces thermo mechanical stresses while allowing for increased heat dissipation is essential for increasing efficiency and reliability. Yet, new packaging structures and configurations are in many ways limited by the current solder and wirebonding attachment technologies. A Low Temperature Joining Technology (LTJT) like that of the sintered silver die attachment is very well suited for fabrication of intricate geometries and the integration of advanced materials. In addition to the enhanced reliability and superior electrical and thermal conductivity, sintered silver has a low homologous temperature which is well suited to the multi-step manufacturing of 3D electronic packages.

In this presentation we present an overview of the challenges facing the power electronics packaging in electric vehicles. These challenges are representative of most electric conversion systems regardless of application. We then present a double sided packaging solution which will increase heat dissipation, allow for enhanced forced cooling and integrate well into full inverter configurations. The design, fabrication, and benefits of this package using nanosilver paste will be discussed in detail. Finally, preliminary package characterization techniques and results will be reviewed.

Bio

David Berry is a PhD candidate in the MSE Department at Virginia Tech. He received both B.S. and M.S. degrees from Virginia Tech Materials Science & Engineering Department. He is also a member of the Center for Power Electronics (CPES) at Virginia Tech. He is advised by Dr. G.Q. Lu (MSE, ECE) and Dr. Khai Ngo (ECE). His research focuses on electronic packaging applications and manufacturing.